ET3001 – Digital System Design

Subject Code	ET3001	**Subject Title**	Digital System Design			
Credits	2.0	**Total Hours**	**Lectures**	24 h	**Pre-Requisites**	ET2001
GPA/NGPA	GPA		**Lab/Assignment**	12 h		

Aims: To provide knowledge and experience with design and implementation of digital systems

Learning Outcomes

On successful completion of this module, students are able to:

1. Demonstrate skills in Hardware Description Languages, design and implement sequential systems using RTL Based Approach
2. Demonstrate knowledge of Xilinx ISE for Digital Design
3. Design RTL Based System
4. Identify key stages in designing a processor

Topics

LO 1.	**Demonstrate skills in Hardware Description Languages, design and implement sequential systems using RTL Based Approach [4 h]** Introduction to reconfigurable computing; Circuit specifications using HDL
LO 2.	**Demonstrate knowledge of Xilinx ISE for Digital Design [4 h]** Writing HDL codes and Simulations; Xilinx Core Generator
LO 3.	**Design RTL Based System [8 h]** Introduction to RTL based design; Data paths and controllers
LO 4.	**Identify key stages in designing a processor [8 h]** Features of RISC architecture; Instruction Set Architecture, Hardwired and micro-programmed approach

Practical Work: [2×3 h]

1. Getting Started with Xilinx ISE
2. Xilinx Core Generator

Assignments: 1 Group Project [6 h]

Assessment

a.	Practical Work:	15%
b.	Assignment - Group Project	15%
c.	End Semester Written Exam - 2 h test	70%

Rec. Bks.

1. **Structured Computer Organization** by Andrew S. Tanenbaum
   Publisher: Prentice Hall, 2006 **ISBN**: 81-203-2913-9
2. **Advanced Digital Design with the Verilog HDL** by Micheal D. Ciletti
   Publisher: Prentice Hall Inc, India: 2003 **ISBN:**81-203-2756-X