Lecture – (4) 27/07/2017 Handout – (1)

TABLE 5.1
Unloaded BJT Transistor Amplifiers

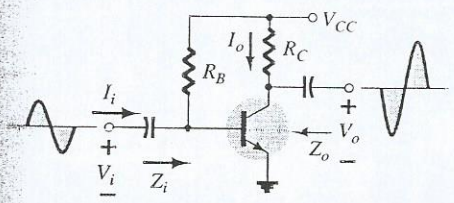
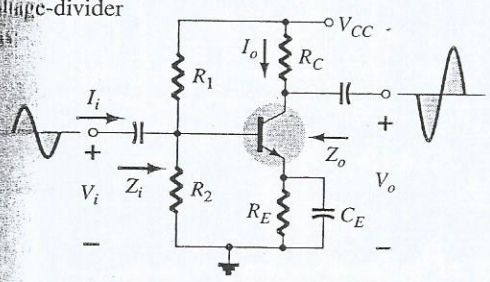
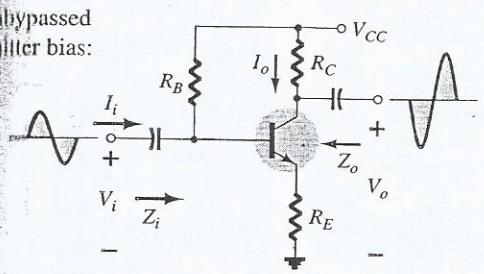
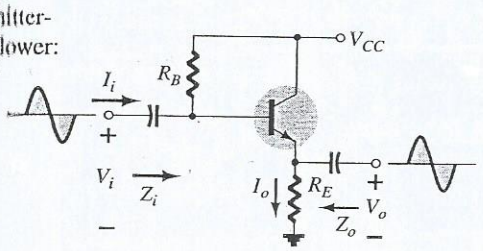
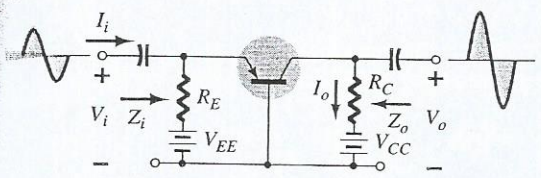
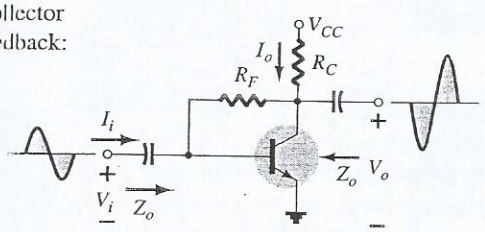
Configuration	Z_i Input Impedance	Z_o Output Impedance	A_v Voltage Gain	A_i Current Gain
Fixed bias: 	Medium (1 kΩ) $= R_B \| \beta r_e$ $\cong \beta r_e$ $(R_B \geq 10\beta r_e)$	Medium (2 kΩ) $= R_C \| r_o$ $\cong R_C$ $(r_o \geq 10R_C)$	High (−200) $= -\frac{(R_C \| r_o)}{r_e}$ $\cong -\frac{R_C}{r_e}$ $(r_o \geq 10R_C)$	High (100) $= \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}$ $\cong \beta$ $(r_o \geq 10R_C, R_B \geq 10\beta r_e)$
Voltage-divider bias: 	Medium (1 kΩ) $= R_1 \| R_2 \| \beta r_e$	Medium (2 kΩ) $= R_C \| r_o$ $\cong R_C$ $(r_o \geq 10R_C)$	High (−200) $= -\frac{R_C \| r_o}{r_e}$ $\cong -\frac{R_C}{r_e}$ $(r_o \geq 10R_C)$	High (50) $= \frac{\beta(R_1 \| R_2) r_o}{(r_o + R_C)(R_1 \| R_2 + \beta r_e)}$ $\cong \frac{\beta(R_1 \| R_2)}{R_1 \| R_2 + \beta r_e}$ $(r_o \geq 10R_C)$
Unbypassed emitter bias: 	High (100 kΩ) $= R_B \| Z_b$ $Z_b \cong \beta(r_e + R_E)$ $\cong R_B \| \beta R_E$ $(R_E \gg r_e)$	Medium (2 kΩ) $= R_C$ (any level of r_o)	Low (−5) $= \frac{R_C}{r_e + R_E}$ $\cong \frac{R_C}{R_E}$ $(R_E \gg r_e)$	High (50) $\cong -\frac{\beta R_B}{R_B + Z_b}$
Emitter-follower: 	High (100 kΩ) $= R_B \| Z_b$ $Z_b \cong \beta(r_e + R_E)$ $\cong R_B \| \beta R_E$ $(R_E \gg r_e)$	Low (20 Ω) $= R_E \| r_e$ $\cong r_e$ $(R_E \gg r_e)$	Low ($\cong$ 1) $= \frac{R_E}{R_E + r_e}$ $\cong 1$	High (−50) $\cong -\frac{\beta R_B}{R_B + Z_b}$
Common-base: 	Low (20 Ω) $= R_E \| r_e$ $\cong r_e$ $(R_E \gg r_e)$	Medium (2 kΩ) $= R_C$	High (200) $\cong \frac{R_C}{r_e}$	Low (−1) $\cong -1$
Collector feedback: 	Medium (1 kΩ) $= \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}}$ $(r_o \geq 10R_C)$	Medium (2 kΩ) $\cong R_C \| R_F$ $(r_o \geq 10R_C)$	High (−200) $\cong -\frac{R_C}{r_e}$ $(r_o \geq 10R_C)$ $(R_F \gg R_C)$	High (50) $= \frac{\beta R_F}{R_F + \beta R_C}$ $\cong \frac{R_F}{R_C}$

TABLE 5.2

BJT Transistor Amplifiers Including the Effect of R_s and R_L

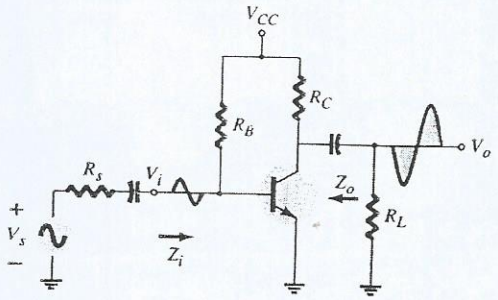
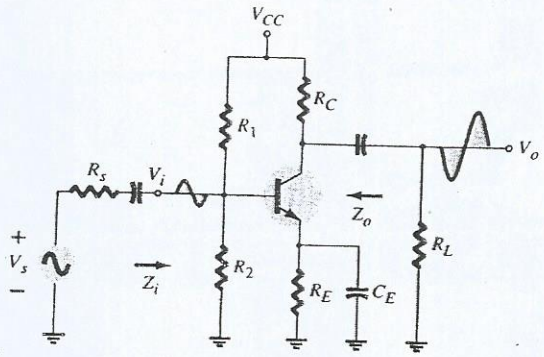
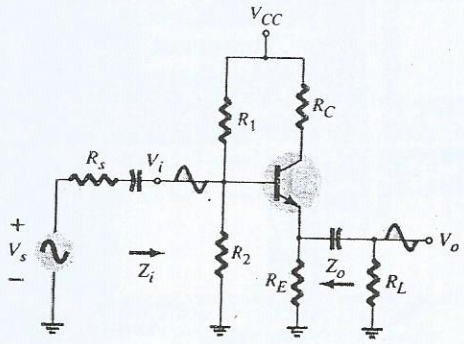
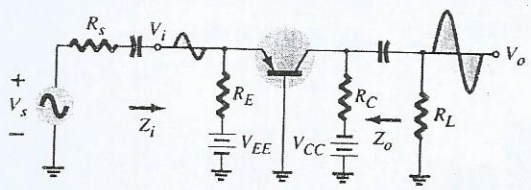
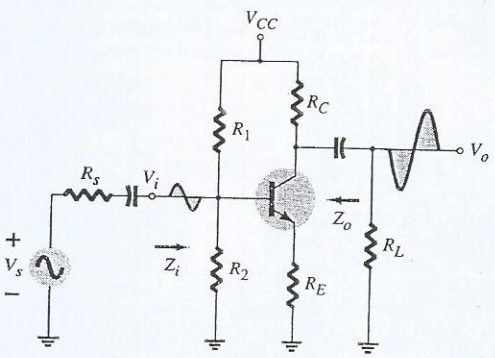
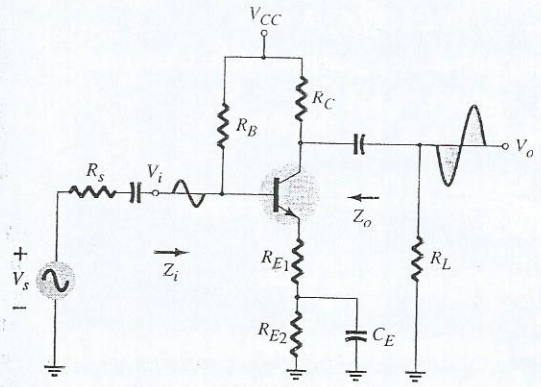
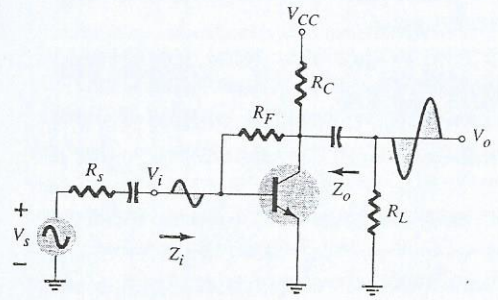
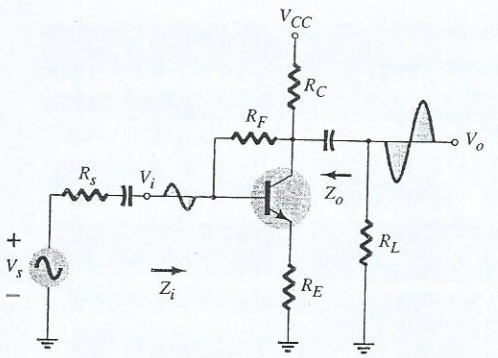
Configuration	$A_{v_L} = V_o/V_i$	Z_i	Z_o
	$\dfrac{-(R_L \| R_C)}{r_e}$	$R_B \| \beta r_e$	R_C
	Including r_o: $\dfrac{-(R_L \| R_C \| r_o)}{r_e}$	$R_B \| \beta r_e$	$R_C \| r_o$
	$\dfrac{-(R_L \| R_C)}{r_e}$	$R_1 \| R_2 \| \beta r_e$	R_C
	Including r_o: $\dfrac{-(R_L \| R_C \| r_o)}{r_e}$	$R_1 \| R_2 \| \beta r_e$	$R_C \| r_o$
	$\cong 1$	$R'_E = R_L \| R_E$ $R_1 \| R_2 \| \beta(r_e + R'_E)$	$R'_s = R_s \| R_1 \| R_2$ $R_E \| \left(\dfrac{R'_s}{\beta} + r_e\right)$
	Including r_o: $\cong 1$	$R_1 \| R_2 \| \beta(r_e + R'_E)$	$R_E \| \left(\dfrac{R'_s}{\beta} + r_e\right)$
	$\cong \dfrac{-(R_L \| R_C)}{r_e}$	$R_E \| r_e$	R_C
	Including r_o: $\cong \dfrac{-(R_L \| R_C \| r_o)}{r_e}$	$R_E \| r_e$	$R_C \| r_o$
	$\dfrac{-(R_L \| R_C)}{R_E}$	$R_1 \| R_2 \| \beta(r_e + R_E)$	R_C
	Including r_o: $\dfrac{-(R_L \| R_C)}{R_E}$	$R_1 \| R_2 \| \beta(r_e + R_e)$	$\cong R_C$

TABLE 5.2 (Continued)

BJT Transistor Amplifiers Including the Effect of R_s *and* R_L

Configuration	$A_{v_L} = V_o/V_i$	Z_i	Z_o
	$\dfrac{-(R_L\|R_C)}{R_{E_1}}$	$R_B\|\beta(r_e + R_{E_1})$	R_C
	Including r_o: $\dfrac{-(R_L\|R_C)}{R_{E_t}}$	$R_B\|\beta(r_e + R_E)$	$\cong R_C$
	$\dfrac{-(R_L\|R_C)}{r_e}$	$\beta r_e\|\dfrac{R_F}{\|A_v\|}$	R_C
	Including r_o: $\dfrac{-(R_L\|R_C\|r_o)}{r_e}$	$\beta r_e\|\dfrac{R_F}{\|A_v\|}$	$R_C\|R_F\|r_o$
	$\dfrac{-(R_L\|R_C)}{R_E}$	$\beta R_E\|\dfrac{R_F}{\|A_v\|}$	$\cong R_C\|R_F$
	Including r_o: $\cong\dfrac{-(R_L\|R_C)}{R_E}$	$\cong \beta R_E\|\dfrac{R_F}{\|A_v\|}$	$\cong R_C\|R_F$

E_{Th} is the open-circuit voltage between the output terminals, identified as V_o. However,

$$A_{v_{\text{NL}}} = \frac{V_o}{V_i}$$

and

$$V_o = A_{v_{\text{NL}}} V_i$$

so that

$$\boxed{E_{\text{Th}} = A_{v_{\text{NL}}} V_i} \qquad (5.82)$$

Substituting the Thévenin equivalent circuit between the output terminals results in the output configuration of Fig. 5.63. For the input circuit the parameters V_i and I_i are related by $Z_i = R_i$, permitting the use of R_i to represent the input circuit. Because our present interest is in BJT and FET amplifiers, both Z_o and Z_i can be represented by resistive elements.

Before continuing, let us check the results of Fig. 5.63 by finding Z_o and $A_{v_{\text{NL}}}$ in the usual manner. To find Z_o, V_i is set to zero, resulting in $A_{v_{\text{NL}}} V_i = 0$, permitting a short-circuit

Eq. (5.85): $$A_{v_s} = \frac{Z_{i_1}}{Z_{i_1} + R_s} A_{v_T} = \frac{(10\,\text{k}\Omega)(101.20)}{10\,\text{k}\Omega + 1\,\text{k}\Omega} = \mathbf{92}$$

c. Eq. (5.94): $$A_{i_T} = -A_{v_T}\frac{Z_{i_1}}{R_L} = -(101.20)\left(\frac{10\,\text{k}\Omega}{8.2\,\text{k}\Omega}\right) = \mathbf{-123.41}$$

d. Eq. (5.85): $$V_i = \frac{Z_{i_{CB}}}{Z_{i_{CB}} + R_s} V_s = \frac{26\,\Omega}{26\,\Omega + 1\,\text{k}\Omega} V_s = 0.025\,V_s$$

and $$\frac{V_i}{V_s} = 0.025 \quad \text{with} \quad \frac{V_o}{V_i} = 147.97 \quad \text{from above}$$

and $$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s}\cdot\frac{V_o}{V_i} = (0.025)(147.97) = \mathbf{3.7}$$

In total, therefore, the gain is about 25 times greater with the emitter-follower configuration to draw the signal to the amplifier stages. Note, however, that it is also important that the output impedance of the first stage is relatively close to the input impedance of the second stage, otherwise the signal would have been "lost" again by the voltage-divider action.

RC-Coupled BJT Amplifiers

One popular connection of amplifier stages is the *RC*-coupled variety shown in Fig. 5.71 in the next example. The name is derived from the capacitive coupling capacitor C_c and the fact that the load on the first stage is an *RC* combination. The coupling capacitor isolates the two stages from a dc viewpoint but acts as a short-circuit equivalent for the ac response. The input impedance of the second stage acts as a load on the first stage, permitting the same approach to the analysis as described in the last two sections.

EXAMPLE 5.15

a. Calculate the no-load voltage gain and output voltage of the *RC*-coupled transistor amplifiers of Fig. 5.71.
b. Calculate the overall gain and output voltage if a 4.7 kΩ load is applied to the second stage, and compare to the results of part (a).
c. Calculate the input impedance of the first stage and the output impedance of the second stage.

CE – CE Cascade

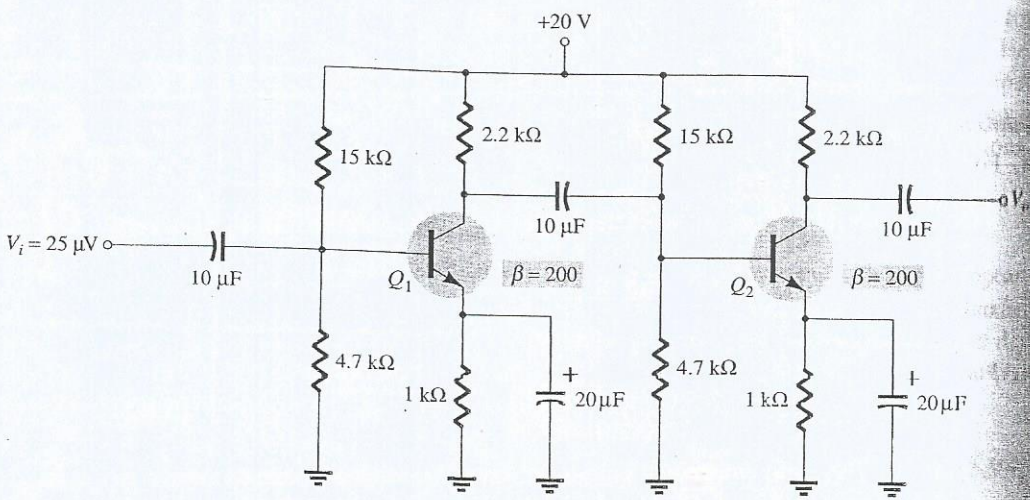


FIG. 5.71
RC-coupled BJT amplifier for Example 5.15.

Solution:

a. The dc bias analysis results in the following for each transistor:

$$V_B = 4.7\,\text{V}, \quad V_E = 4.0\,\text{V}, \quad V_C = 11\,\text{V}, \quad I_E = 4.0\,\text{mA}$$

At the bias point,

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4\text{ mA}} = 6.5\ \Omega$$

The loading of the second stage is

$$Z_{i_2} = R_1 \| R_2 \| \beta r_e$$

which results in the following gain for the first stage:

$$A_{v_1} = -\frac{R_C \| (R_1 \| R_2 \| \beta r_e)}{r_e}$$

$$= -\frac{(2.2\,\text{k}\Omega) \| [15\,\text{k}\Omega \| 4.7\,\text{k}\Omega \| (200)(6.5\ \Omega)]}{6.5\ \Omega}$$

$$= -\frac{665.2\ \Omega}{6.5\ \Omega} = -102.3$$

For the unloaded second stage the gain is

$$A_{v_{2(\text{NL})}} = -\frac{R_C}{r_e} = -\frac{2.2\text{ k}\Omega}{6.5\ \Omega} = -338.46$$

resulting in an overall gain of

$$A_{v_{T(\text{NL})}} = A_{v_1} A_{v_{2(\text{NL})}} = (-102.3)(-338.46) \cong \mathbf{34.6 \times 10^3}$$

The output voltage is then

$$V_o = A_{v_{T(\text{NL})}} V_i = (34.6 \times 10^3)(25\ \mu\text{V}) \cong \mathbf{865\ mV}$$

b. The overall gain with the 10-kΩ load applied is

$$A_{v_T} = \frac{V_o}{V_i} = \frac{R_L}{R_L + Z_o} A_{v_{T(\text{NL})}} = \frac{4.7\text{ k}\Omega}{4.7\text{ k}\Omega + 2.2\,\text{k}\Omega}(34.6 \times 10^3) \cong \mathbf{23.6 \times 10^3}$$

which is considerably less than the unloaded gain because R_L is relatively close to R_C.

$$V_o = A_{v_T} V_i$$

$$= (23.6 \times 10^3)(25\ \mu\text{V})$$

$$= \mathbf{590\ mV}$$

c. The input impedance of the first stage is

$$Z_{i_1} = R_1 \| R_2 \| \beta r_e = 4.7\,\text{k}\Omega \| 15\,\text{k}\Omega \| (200)(6.5\ \Omega) = \mathbf{953.6\ \Omega}$$

whereas the output impedance for the second stage is

$$Z_{o_2} = R_C = \mathbf{2.2\,k\Omega}$$

Cascode Connection

The cascode configuration has one of two configurations. In each case the collector of the leading transistor is connected to the emitter of the following transistor. One possible arrangement appears in Fig. 5.72; the second is shown in Fig. 5.73 in the following example. The

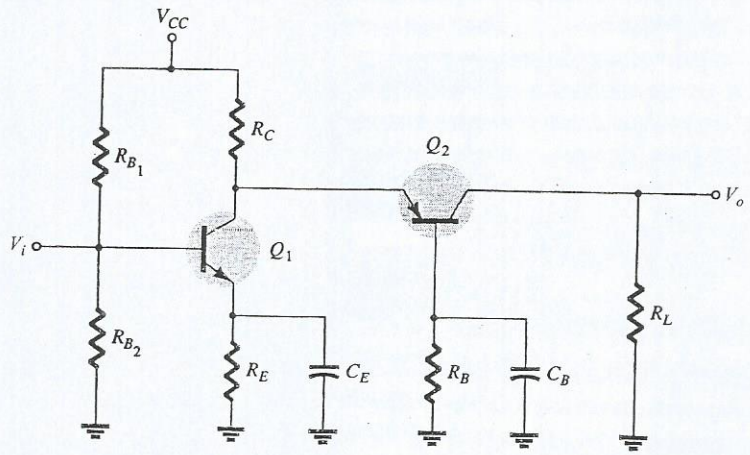


FIG. 5.72
Cascode configuration.

CE - CB Cascode

5.11 HYBRID π MODEL

The last transistor model to be introduced is the hybrid π model, which includes parameters that do not appear in the other two models primarily to provide a more accurate model for high-frequency effects. For lower frequencies approximations to the model can be made with the result that the r_e model introduced earlier will result. The hybrid π model appears in Fig. 5.123 with all the parameters necessary for a full-frequency analysis.

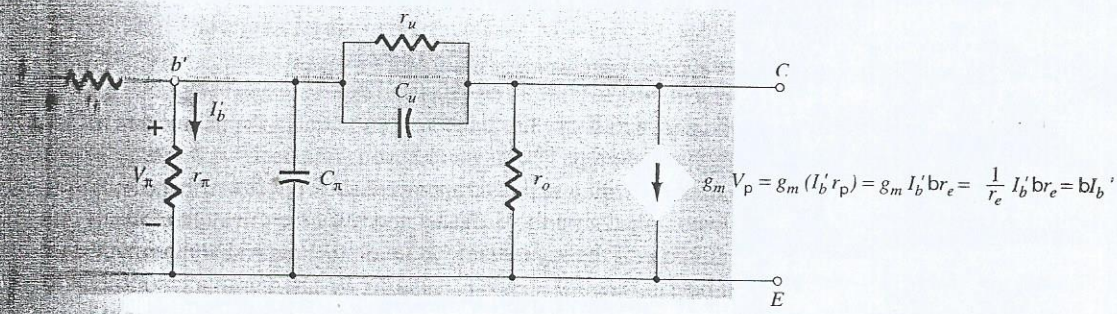


FIG. 5.123
Giacoletto (or hybrid π) high-frequency transistor small-signal ac equivalent circuit.

All the capacitors that appear in Fig. 5.123 are stray parasitic capacitors between the various junctions of the device. They are all capacitive effects that really only come into play at high frequencies. For low to mid-frequencies their reactance is very large, and they can be considered open circuits. The capacitor C_u is usually just a few picofarads (pF) to a few tens of picofarads, whereas the capacitance C_u typically extends from less than 1 pF to a few picofarads. The resistance r_b includes the base contact, base bulk, and base spreading resistance levels. The first is due to the actual connection to the base. The second includes the resistance from the external terminal to the active region of the transistor, and the last is the actual resistance within the active base region. It is typically a few ohms to tens of ohms. The resistors r_π, r_u, and r_o are the resistances between the indicated terminals of the device when the device is in the active region. The resistance r_π (using the symbol π to agree with the hybrid π terminology) is simply βr_e as introduced for the common-emitter r_e model. The resistance r_u (the subscript u refers to the *union* it provides between collector and base terminals) is a very large resistance and provides a feedback path from output to input circuits in the equivalent model. It is typically larger than βr_o, which places it in the megohm range. The output resistance r_o is the output resistance normally appearing across an applied load. Its value, which typically lies between 5 kΩ and 40 kΩ, is determined from the hybrid parameter h_{oe}.

It is important to note in Fig. 5.123 that the controlled source can be a voltage-controlled current source (VCCS) or a current-controlled current source (CCCS), depending on the parameters employed.

For the broad range of low- to mid-frequency analysis, the effect of the stray capacitive effects can be ignored due to the very high reactance levels associated with each. The resistance r_b is usually so small it can be replaced by a short-circuit equivalent, and the resistance r_u is usually so large it can be ignored for most applications. The result is an equivalent network similar to the r_e common-emitter model introduced earlier.

Because the use of the model is totally dependent on finding the parameter values for the equivalent network, it is important to be aware of the following relationships to extract the parameter values from the data typically provided:

$$r_\pi = \beta r_e \tag{5.162}$$

$$g_m = \frac{1}{r_e} \tag{5.163}$$

$$r_o = \frac{1}{h_{oe}} \tag{5.164}$$

$$h_{re} = \frac{r_\pi}{r_\pi + r_u} \cong \frac{r_\pi}{r_\mu} \tag{5.165}$$

The equivalence between the two sources of Fig. 5.123 is demonstrated in the figure using Eqs. (5.162) and (5.163).

The hybrid π model will not appear in the small-signal analysis of this chapter because it is primarily used to investigate high-frequency effects. It will appear again in the discussion of high-frequency effects in Chapter 9.

5.23 VARIATIONS OF TRANSISTOR PARAMETERS

A variety of curves can be drawn to show the variations of the transistor parameters with temperature, frequency, voltage, and current. The most interesting and useful at this stage of the development include the variations with junction temperature and collector voltage and current.

The effect of the collector current on the r_e model and hybrid equivalent model is shown in Fig. 5.124. Take careful note of the logarithmic scale on the vertical and horizontal axes. Logarithmic scales will be examined in detail in Chapter 9. The parameters have all been normalized to unity so that the relative change in magnitude with collector current can easily be determined. On each set of curves, such as in Figs. 5.124 to 5.126, the operating point at which the parameters were determined is always indicated. For this particular situation, the quiescent point is at the fairly typical values of $V_{CE} = 5.0$ V and $I_C = 1.0$ mA. Because the frequency and temperature of operation also affect the parameters, these quantities are also indicated on the curves. Figure 5.124 shows the variation of the parameters with collector current. Note that at $I_C = 1$ mA the value of all the parameters has been normalized to 1 on the vertical axis. The result is that the magnitude of each parameter is compared to the values at the defined operating point. Because manufacturers typically use the hybrid parameters for plots of this type, they are the curves of choice in Fig. 5.124. However, to broaden the use of the curves the r_e and hybrid π equivalent parameters have also been added.

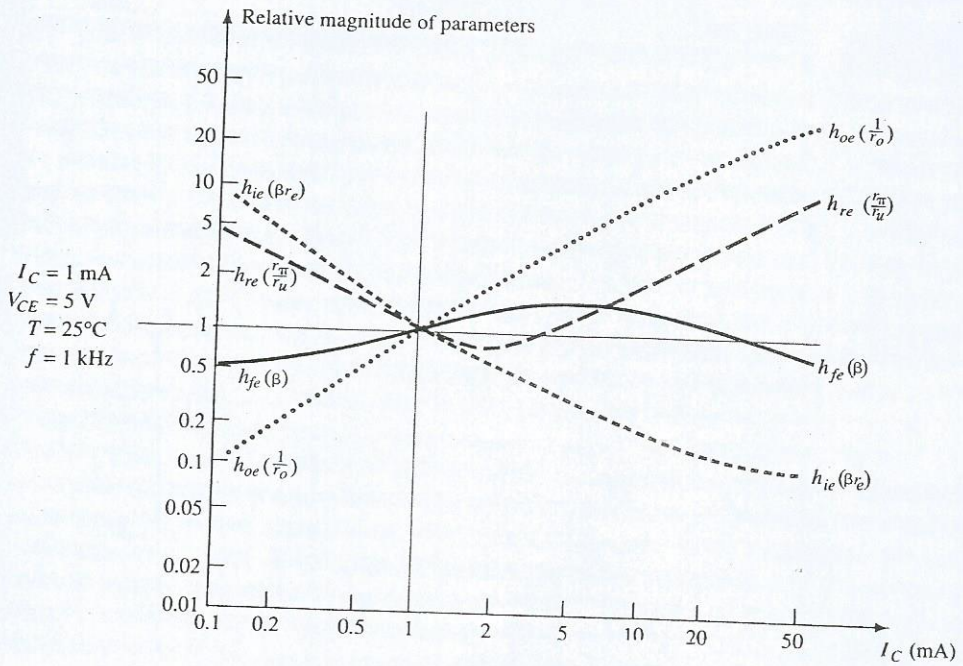


FIG. 5.124
Hybrid parameter variations with collector current.

At first glance it is particularly interesting to note that:

The parameter $h_{fe}(\beta)$ varies the least of all the parameters of a transistor equivalent circuit when plotted against variations in collector current.

Figure 5.124 clearly reveals that for the full range of collector current the parameter $h_{fe}(\beta)$ varies from 0.5 of its Q-point value to a peak of about 1.5 times that value at a current of about 6 mA. For a transistor with a β of 100, it therefore varies from about 50 to 150.

This seems like quite a bit, but look at h_{oe}, which jumps to almost 40 times its Q-point value at a collector current of 50 mA.

Figure 5.124 also shows that $h_{oe}(1/r_o)$ and $h_{ie}(\beta r_e)$ vary the most for the chosen current range. The parameter h_{ie} varies from about 10 times its Q-point value down to about one tenth of Q-point the value at 50 mA. This variation, however, should be expected because we know that the value of r_e is directly related to the emitter current by $r_e = 26\,\text{mV}/I_E$. As $I_E\,(= I_C)$ increases, the value of r_e and therefore βr_e will decrease, as shown in Fig. 5.124.

Keep in mind as you review the curve of h_{oe} versus current that the actual output resistance r_o is $1/h_{oe}$. Therefore, as the curve increases with current, the value of r_o becomes less and less. Because r_o is a parameter that normally appears in parallel with the applied load, decreasing values of r_o can become a critical problem. The fact that r_o has dropped to almost 1/40 of its value at the Q-point could spell a real reduction in gain at 50 mA.

The parameter h_{re} varies quite a bit, but because its Q-point value is usually small enough to permit ignoring its effect, it is a parameter that is only of concern for collector currents that are much less, or quite a bit more, than the Q-point level.

This may seem like an extensive description of a set of characteristic curves. However, experience has revealed that graphs of this nature are too often reviewed without taking the time to fully appreciate the broad impact of what they are providing. These plots reveal a lot of information that could be extremely useful in the design process.

Figure 5.125 shows the variation in magnitude of the parameters due to changes in collector-to-emitter voltage. This set of curves is normalized at the same operating point as the curves of Fig. 5.124 to permit comparisons between the two. In this case, however, the vertical scale is in percent rather than whole numbers. The 200% level defines a set of parameters twice that at the 100% level. A level of 1000% would reflect a 10:1 change. Note that h_{fe} and h_{ie} are relatively steady in magnitude with variations in collector-to-emitter voltage, whereas for changes in collector current the variation is a great deal more significant. In other words, if you want a parameter such as $h_{ie}(\beta r_e)$ to remain fairly steady, keep the variation of I_C to a minimum while worrying less about variations in the collector-to-emitter voltage. The variation of h_{oe} and h_{ie} remains significant for the indicated range of collector-to-emitter voltage.

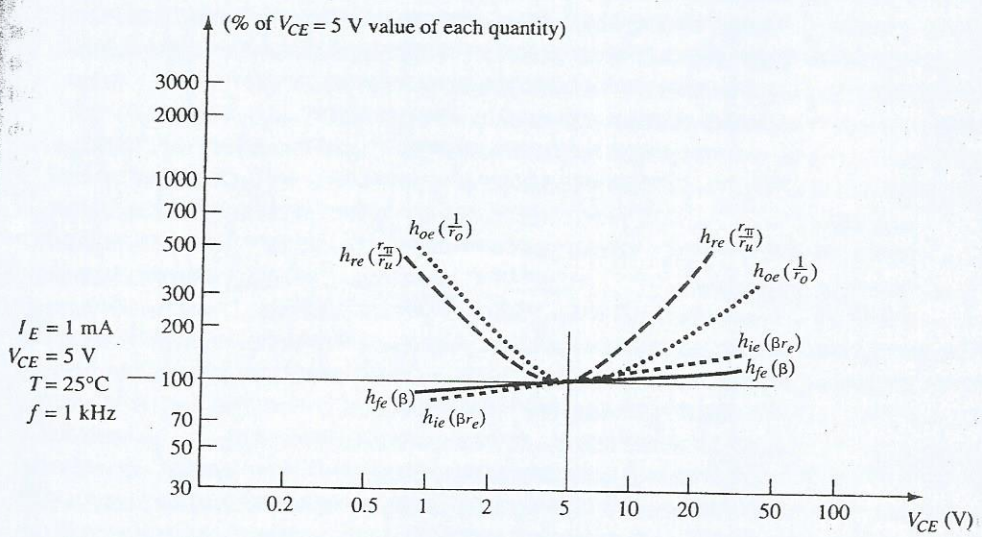


FIG. 5.125

Hybrid parameter variations with collector–emitter potential.

In Fig. 5.126, the variation in parameters is plotted for changes in junction temperature. The normalization value is taken to be room temperature, $T = 25°\text{C}$. The horizontal scale is now a linear scale rather than the logarithmic scale employed in the two previous figures. In general:

All the parameters of a hybrid transistor equivalent circuit increase with temperature.

However, again keep in mind that the actual output resistance r_o is inversely related to h_{oe}, so its value drops with an increase in h_{oe}. The greatest change is in h_{ie}, although note that the range of the vertical scale is considerably less than in the other plots. At a temperature

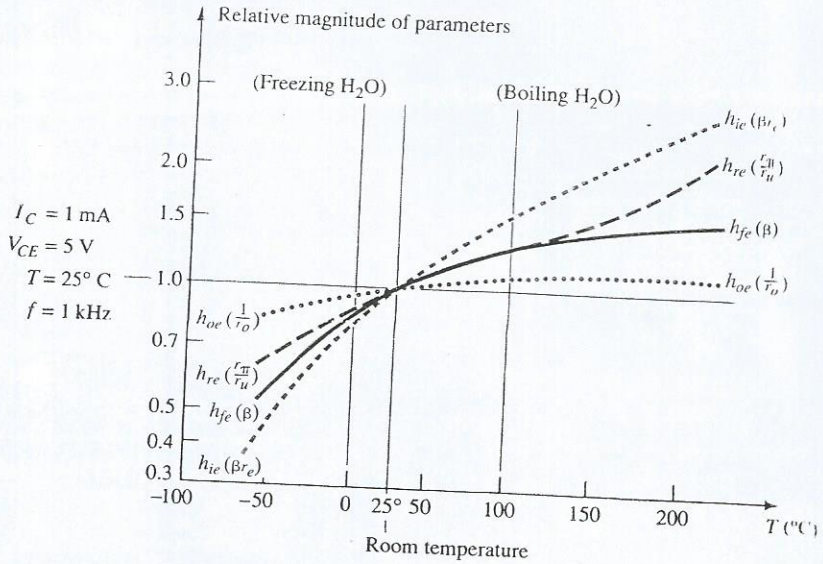


FIG. 5.126
Hybrid parameter variations with temperature.

of 200°C the value of h_{ie} is almost 3 times its Q-point value, but in Fig. 5.124 parameter jumped to almost 40 times the Q-point value.

Of the three parameters, therefore, the variation in collector current has by far the greatest effect on the parameters of a transistor equivalent circuit. Temperature is always a factor, but the effect of the collector current can be significant.

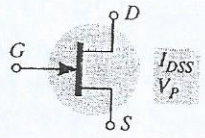
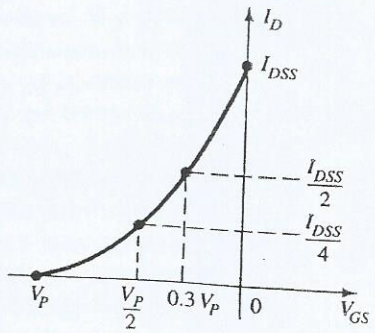
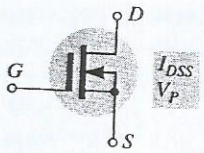
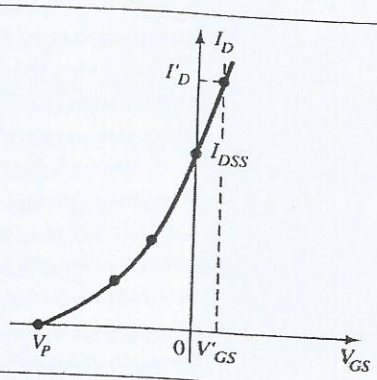
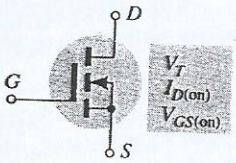
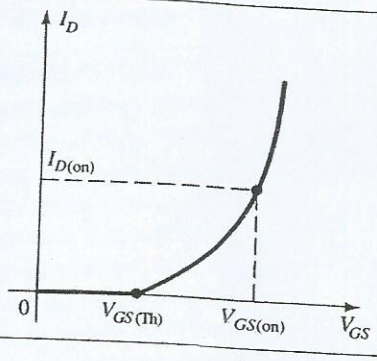
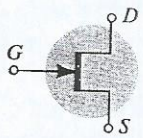
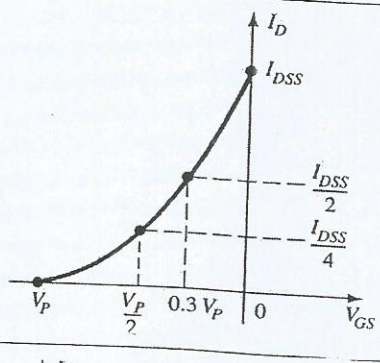
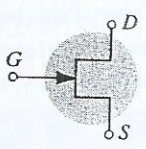
5.24 TROUBLESHOOTING

Although the terminology *troubleshooting* suggests that the procedures to be described are designed simply to isolate a malfunction, it is important to realize that the same techniques can be applied to ensure that a system is operating properly. In any case, the testing, checking, and isolating procedures require an understanding of what to expect at various points in the network in both the dc and ac domains. In most cases, a network operating correctly in the dc mode will also behave properly in the ac domain. In addition, a network providing the expected ac response is most likely biased as planned. In a typical laboratory setting, both the dc and ac supplies are applied and the ac response at various points in the network is checked with an oscilloscope as shown in Fig. 5.127. Note that the black (gnd) lead of the oscilloscope is connected directly to ground and the red lead is moved from point to point in the network, providing the patterns appearing in Fig. 5.127. The vertical channels are set in the ac mode to remove any dc component associated with the voltage at a particular point. The small ac signal applied to the base is amplified to the level appearing from collector to ground. Note the difference in vertical scales for the two voltages. There is no ac response at the emitter terminal due to the short-circuit characteristics of the capacitor at the applied frequency. The fact that v_o is measured in volts and v_i in millivolts suggests a sizable gain for the amplifier. In general, the network appears to be operating properly. If desired, the dc mode of the multimeter could be used to check V_{BE} and the levels of V_B, V_{CE}, and V_E to review whether they lie in the expected range. Of course, the oscilloscope can also be used to compare dc levels simply by switching to the dc mode for each channel.

A poor ac response can be due to a variety of reasons. In fact, there may be more than one problem area in the same system. Fortunately, however, with time and experience, the probability of malfunctions in some areas can be predicted, and an experienced person can isolate problem areas fairly quickly.

In general, there is nothing mysterious about the general troubleshooting process. If you decide to follow the ac response, it it good procedure to start with the applied signal and progress through the system toward the load, checking critical points along the way. An unexpected response at some point suggests that the network is fine up to that area, thereby

TABLE 6.2
Field Effect Transistors

Type	Symbol and Basic Relationships	Transfer Curve	Input
JFET (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	 	
MOSFET depletion type (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	 	
MOSFET enhancement type (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = k\,(V_{GS} - V_{GS\,(Th)})^2$ $k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS\,(Th)})^2}$	 	
MESFET depletion type (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ $I_G = 0\text{ A}, I_D = I_S$	 	
MESFET enhancement type (*n*-channel)	 $I_D = k\,(V_{GS} - V_{GS\,(Th)})^2$ $k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS\,(Th)})^2}$